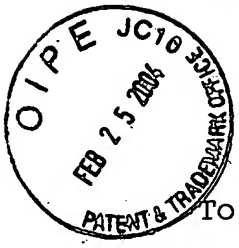
IME-02-021



February 18, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/727,201 12/03/03

Kang Joon Mo et al.

METHOD OF FABRICATING OPTICAL WAVEGUIDE DEVICES WITH SMOOTH AND FLAT DIELECTRIC INTERFACES

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 23, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date Stephen B. Ackerman 2/23/04

U.S. Patent 5,199,092 to Stegmueller, "Optoelectronic Device for Coupling Between Different Dimensioned Waveguides," describes an optical waveguide device.

U.S. Patent 4,954,459 to Avanzino et al., "Method of Planarization of Topologies in Integrated Circuit Structures," describes a planarization method using a sacrificial layer.

U.S. Patent 5,510,652 to Burke et al., "Polishstop Planarization Structure," describes a chemical mechanical polishing (CMP) method using differing polish rates.

The following two U.S. Patents describe planarization methods using both etching and CMP:

1) U.S. Patent 5,863,828 to Snyder, "Trench Planarization Technique."

2) U.S. Patent 5,851,899 to Weigand, "Gapfill and Planarization Process for Shallow Trench Isolation."

U.S. 6,258,711 to Laursen, "Sacrificial Deposit to Improve Damascene Pattern Planarization in Semiconductor Wafers," describes a CMP process with a sacrificial layer that polishes at a different rate than the fill layer to be planarized.

The Christian Laurent-Lund et al., article entitled "PECVD Grown Multiple Core Planar Waveguides with Extremely Low Interface Reflections and Losses," IEEE Photonics Technology Letters, Vol. 10, No. 10, pp. 14311-1433, Oct. 1998, discloses a method of optical waveguide device fabrication using planarization by reverse masking and precise etching.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
IME-02-021	10/727,201
Applicant: Kang Joon Mo et al.	
Filing Date: 12/03/03	Group Art Unit

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5199092	3/30/93	Stegmueller	385	50	1/31/92
	4954459	9/4/90	Avanzino et al.	437	228	7/3/89
	5510652	4/23/96	Burke et al.	257	752	10/6/94
	5863828	1/26/99	Snyder	438	437	9/25/96
	5851899	12/22/98	Weigand	438	427	8/8/96
	6258711	7/10/01	Laursen	438	633	4/19/99

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

- "PECVD Growth Multiple Core Planar Waveguides with Extremely Low Interface Reflections and Losses" by Christian Laurent-Lund et al., IEEE Photonics Tech. Letters, Vol.10, No.10, Oct. 1998, pp. 1431-1433.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.